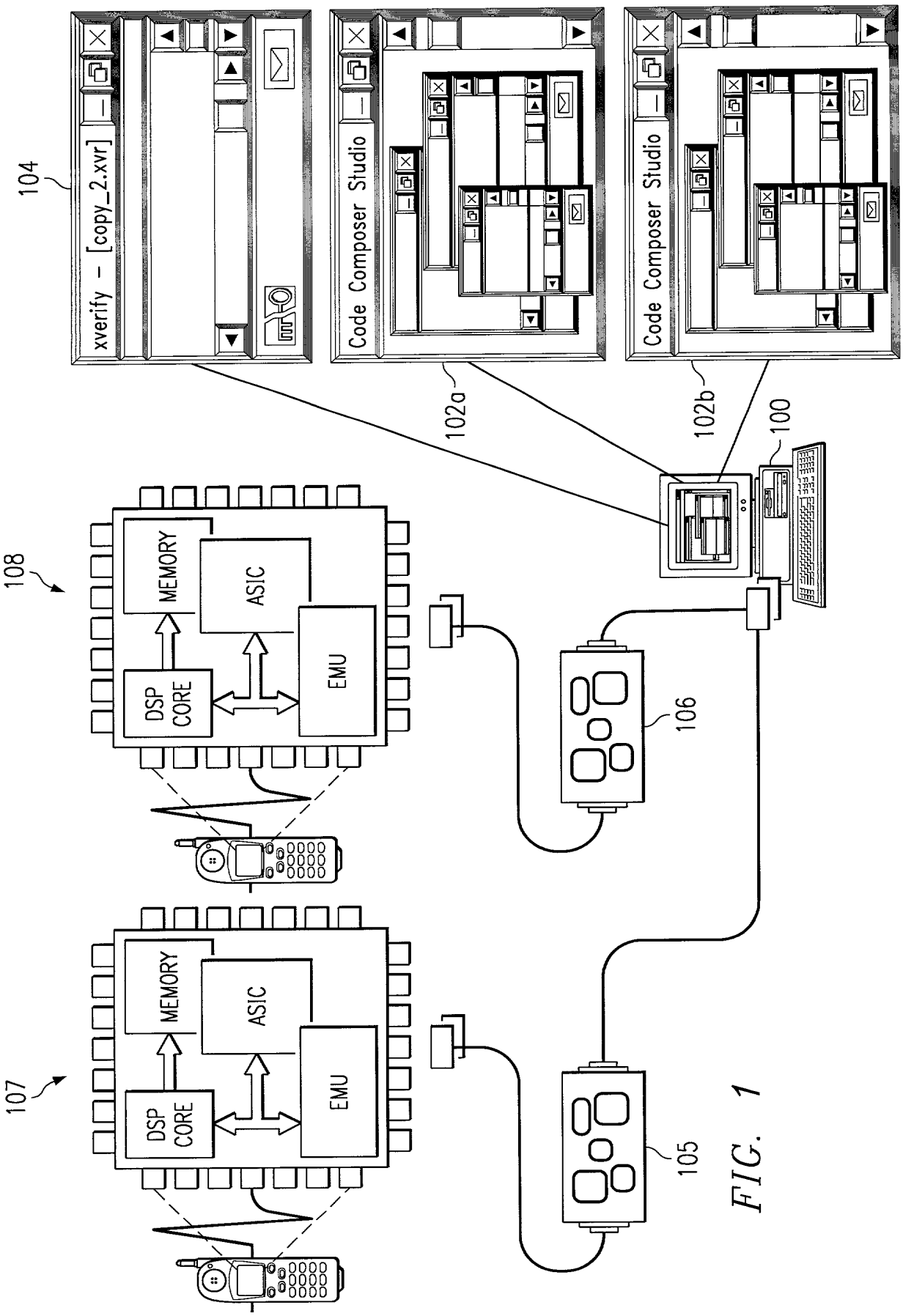


FIG. 1

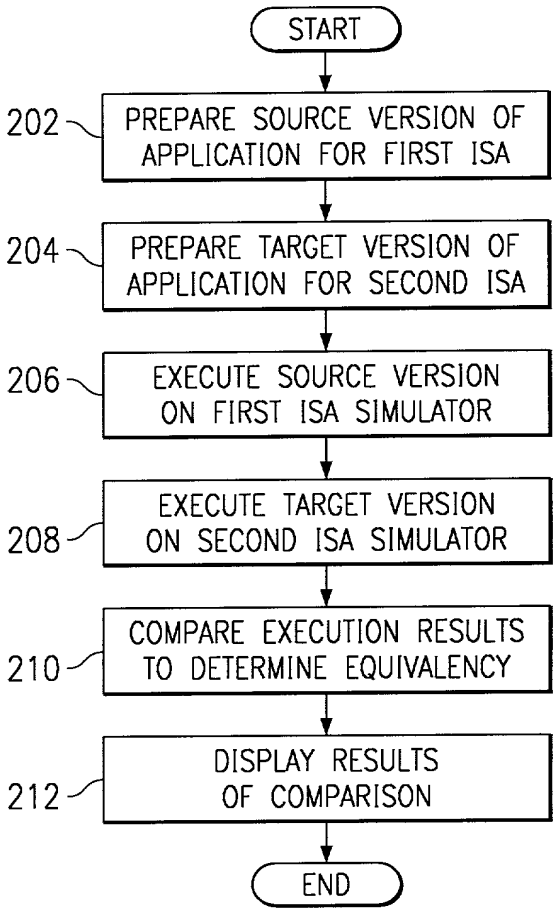


FIG. 2

SOURCE EXECUTION	SOURCE (403)	SOURCE STATE (405)	TARGET EXECUTION	TARGET (404)	TARGET STATE (406)
401	STM data1, AR3	EMPTY	402	MOV data1, AR3	EMPTY
	LD #1, A			MOV #1, AC0	
	NOP			NOP	
	NOP			NOP	
	STL A, *AR3+			MOV AC0<<#0, AR3+	
	NOP			NOP	

FIG. 4a

FIG. 3a

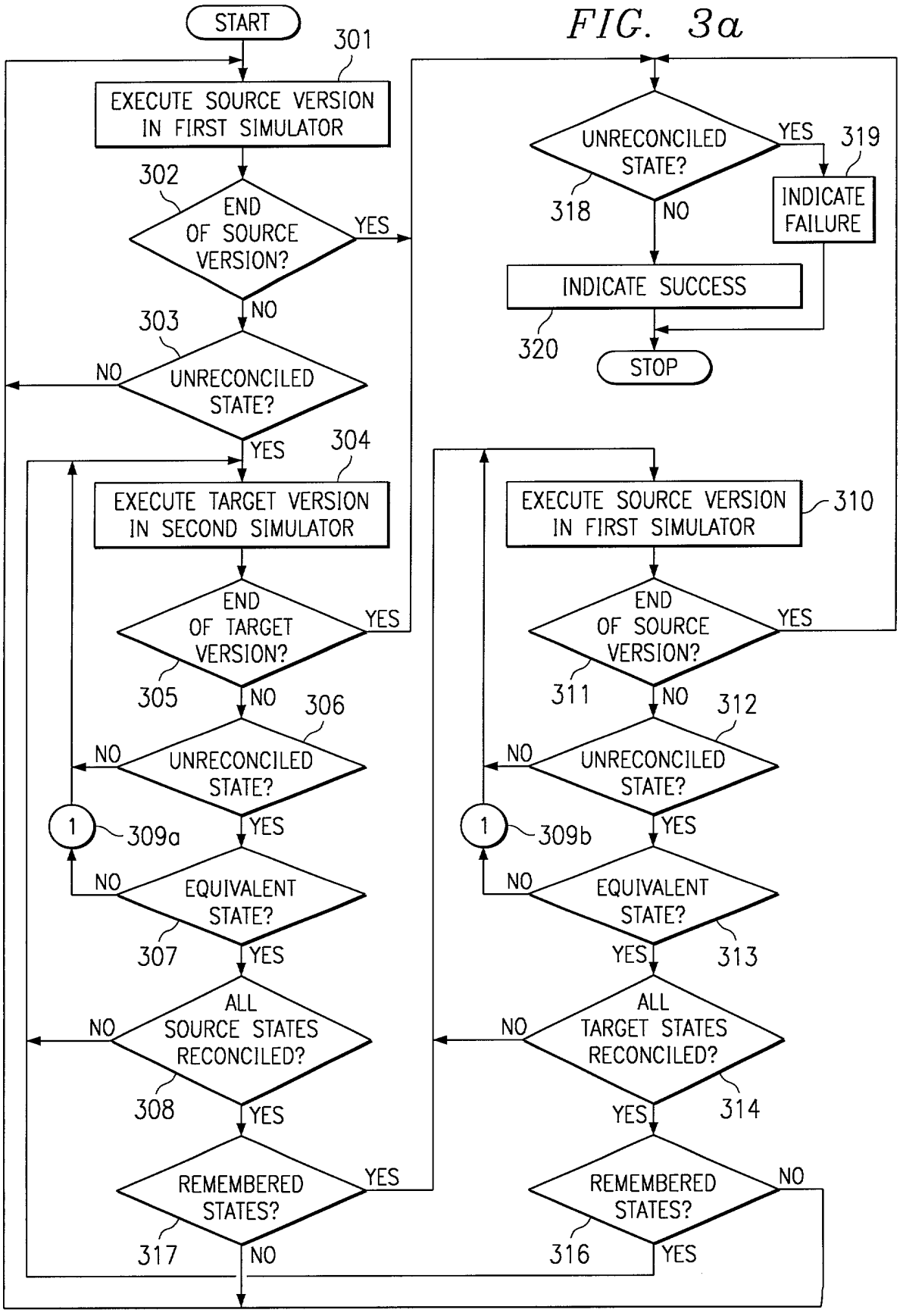

START
301
EXECUTE SOURCE VERSION IN FIRST SIMULATOR
302
END OF SOURCE VERSION?
YES
NO
303
UNRECONCILED STATE?
NO
YES
304
EXECUTE TARGET VERSION IN SECOND SIMULATOR
END OF TARGET VERSION?
YES
305
NO
306
UNRECONCILED STATE?
NO
1
309a
YES
EQUIVALENT STATE?
NO
307
YES
ALL SOURCE STATES RECONCILED?
NO
308
YES
REMEMBERED STATES?
YES
317
NO
UNRECONCILED STATE?
YES
319
318
NO
INDICATE FAILURE
INDICATE SUCCESS
320
STOP
EXECUTE SOURCE VERSION IN FIRST SIMULATOR
310
END OF SOURCE VERSION?
YES
311
NO
312
UNRECONCILED STATE?
NO
1
309b
YES
EQUIVALENT STATE?
NO
YES
313
ALL TARGET STATES RECONCILED?
NO
YES
314
REMEMBERED STATES?
NO
316
YES

FIG. 3b

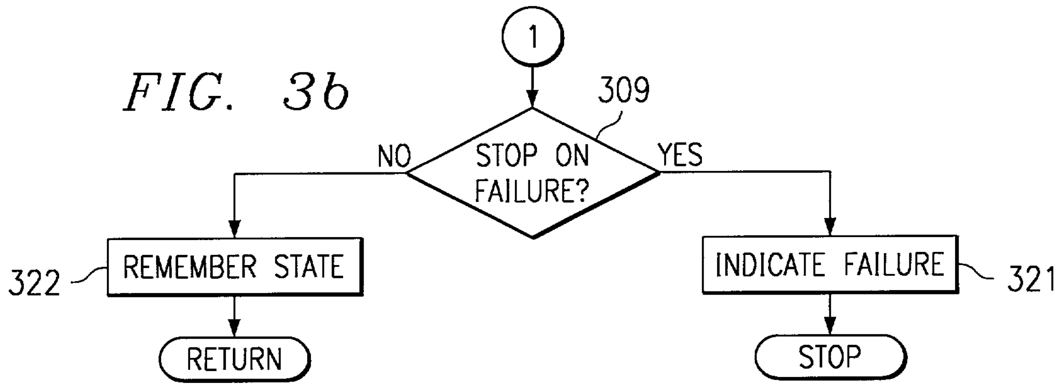


FIG. 4b

SOURCE EXECUTION	SOURCE (403)	SOURCE STATE (405)	TARGET EXECUTION	TARGET (404)	TARGET STATE (406)
	STM data1, AR3		→ 402	MOV data1, AR3	
→ 401	LD #1, A			MOV #1, AC0	
	NOP	AR3=0x800		NOP	EMPTY
	NOP			NOP	
	STL A, *AR3+			MOV AC0<<#0, AR3+	
	NOP			NOP	

FIG. 4c

SOURCE EXECUTION	SOURCE (403)	SOURCE STATE (405)	TARGET EXECUTION	TARGET (404)	TARGET STATE (406)
	STM data1, AR3			MOV data1, AR3	
→ 401	LD #1, A		→ 402	MOV #1, AC0	
	NOP	AR3=0x800		NOP	XAR3= 0x430
	NOP			NOP	
	STL A, *AR3+			MOV AC0<<#0, AR3+	
	NOP			NOP	

SOURCE EXECUTION	SOURCE (403)	SOURCE STATE (405)	TARGET EXECUTION	TARGET (404)	TARGET STATE (406)
	STM data1, AR3	AR3=0x800 A=1		MOV data1, AR3	XAR3= 0x430
	LD #1, A		→	MOV #1, AC0	
→	NOP		402	NOP	
401	NOP			NOP	
	STL A, *AR3+			MOV AC0<<#0, AR3+	
	NOP			NOP	

FIG. 4d

SOURCE EXECUTION	SOURCE (403)	SOURCE STATE (405)	TARGET EXECUTION	TARGET (404)	TARGET STATE (406)
	STM data1, AR3	AR3=0x800 A=1		MOV data1, AR3	XAR3= 0x430 AC0=1
	LD #1, A			MOV #1, AC0	
→	NOP		→	NOP	
401	NOP		402	NOP	
	STL A, *AR3+			MOV AC0<<#0, AR3+	
	NOP			NOP	

FIG. 4e

SOURCE EXECUTION	SOURCE (403)	SOURCE STATE (405)	TARGET EXECUTION	TARGET (404)	TARGET STATE (406)
	STM data1, AR3	AR3=0x800 (*AR3)=1		MOV data1, AR3	XAR3= 0x430
	LD #1, A			MOV #1, AC0	
	NOP		→	NOP	
	NOP		402	NOP	
401	STL A, *AR3+			MOV AC0<<#0, AR3+	
→	NOP			NOP	

FIG. 4f

SOURCE EXECUTION	SOURCE (403)	SOURCE STATE (405)	TARGET EXECUTION	TARGET (404)	TARGET STATE (406)
	STM data1, AR3	AR3=0x800 (*AR3)=1		MOV data1, AR3	XAR3= 0x430 (*XAR3)=1
	LD #1, A			MOV #1, AC0	
	NOP			NOP	
	NOP			NOP	
401	STL A, *AR3+		402	MOV AC0<<#0, AR3+	
→	NOP		→	NOP	

FIG. 4g

FIG. 4h

403 405 404 406

SOURCE EXECUTION	SOURCE	SOURCE STATE	TARGET EXECUTION	TARGET	TARGET STATE
	STM data1, AR3			MOV data1, AR3	
	LD #1, A			MOV #1, AC0	
	NOP	EMPTY		NOP	EMPTY
	NOP			NOP	
401	STL A, *AR3+		402	MOV AC0<<#0, AR3+	
→	NOP		→	NOP	

FIG. 5a

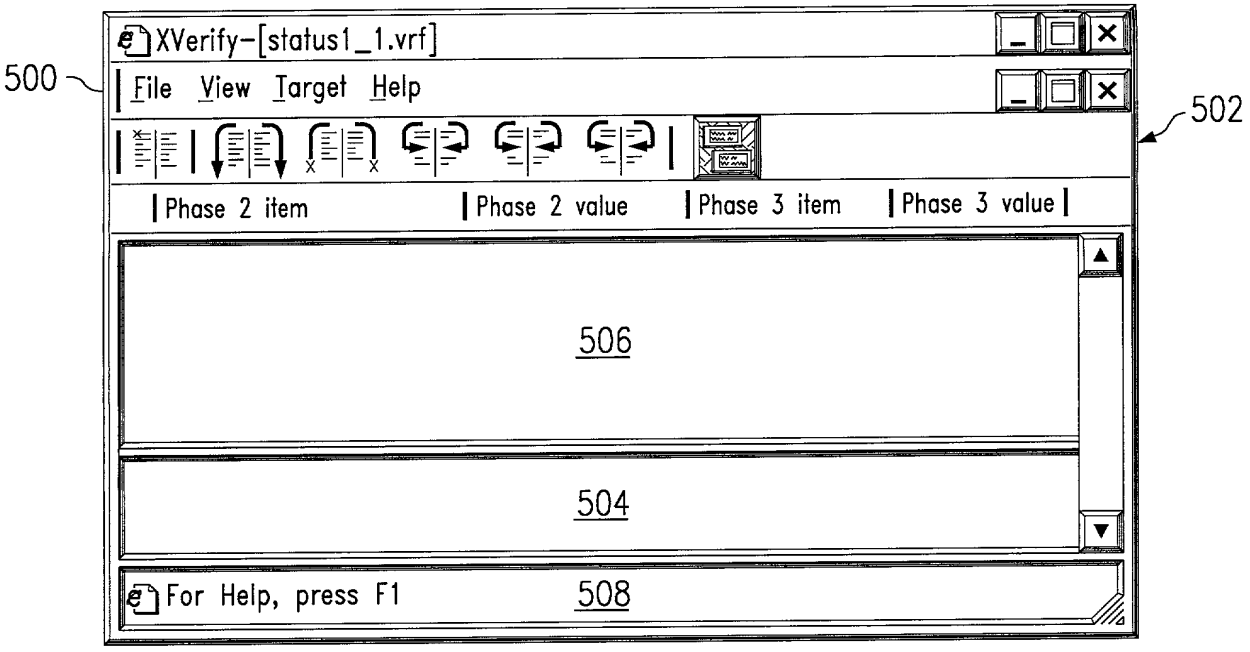


FIG. 5b

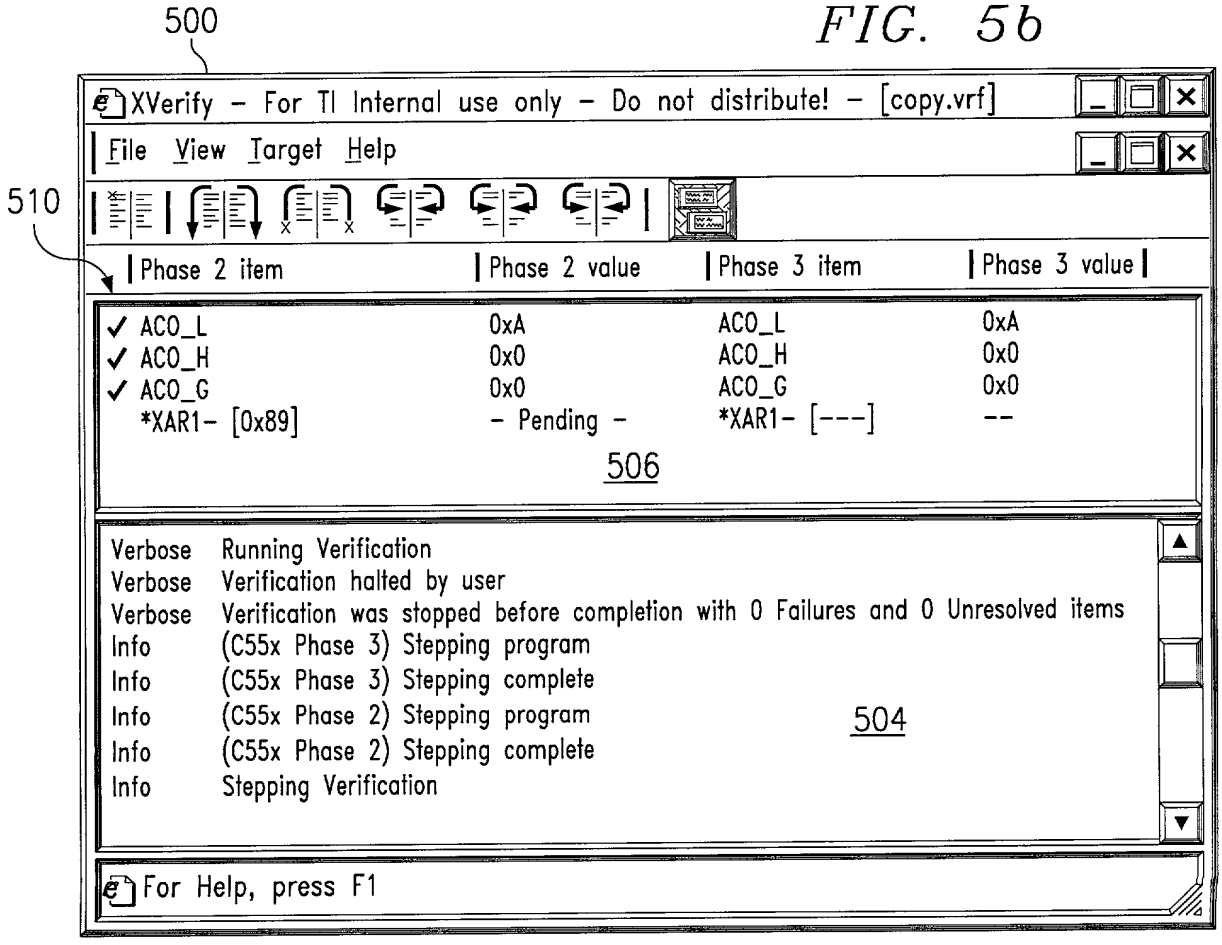


FIG. 6a

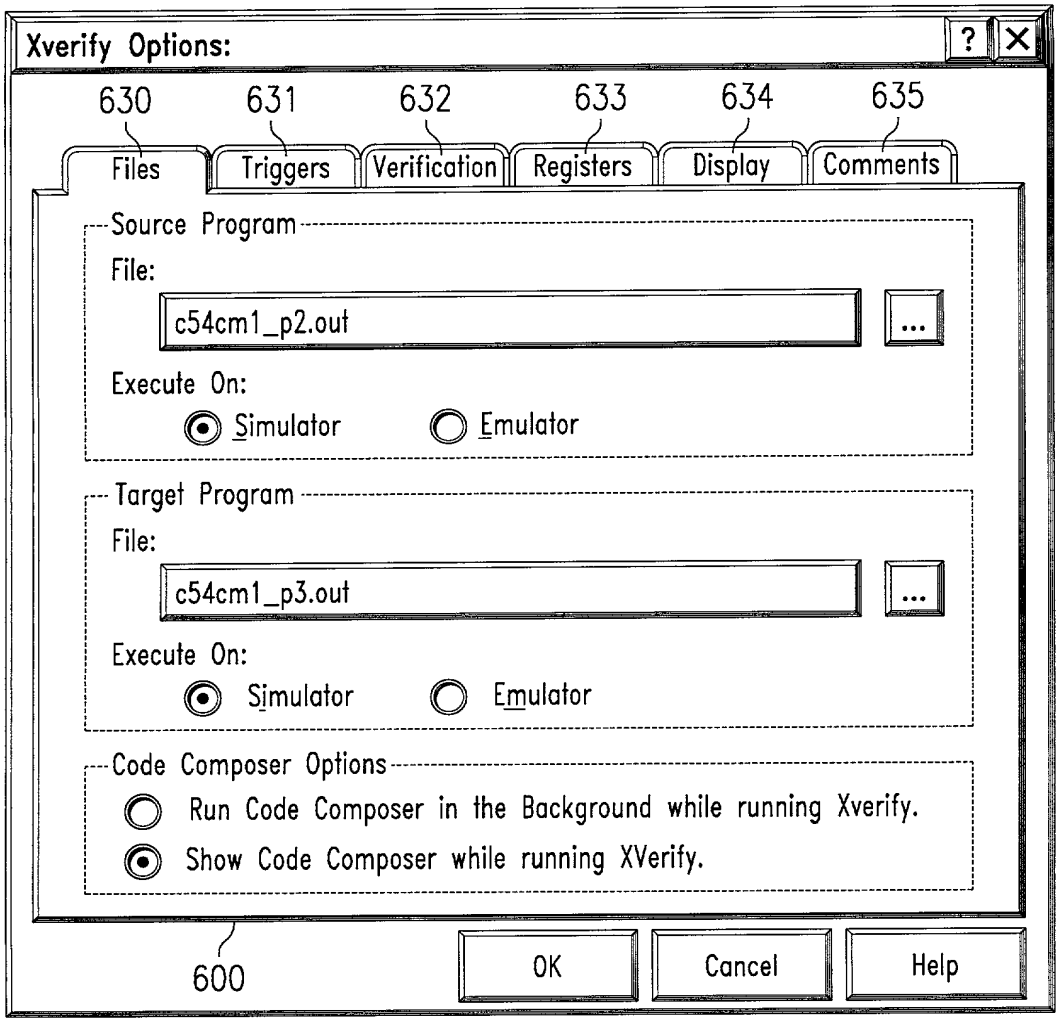

Xverify Options:
630
631
632
633
634
635
Files
Triggers
Verification
Registers
Display
Comments
Source Program
File:
c54cm1_p2.out
...
Execute On:
Simulator
Emulator
Target Program
File:
c54cm1_p3.out
...
Execute On:
Simulator
Emulator
Code Composer Options
Run Code Composer in the Background while running Xverify.
Show Code Composer while running XVerify.
600
OK
Cancel
Help

FIG. 6d

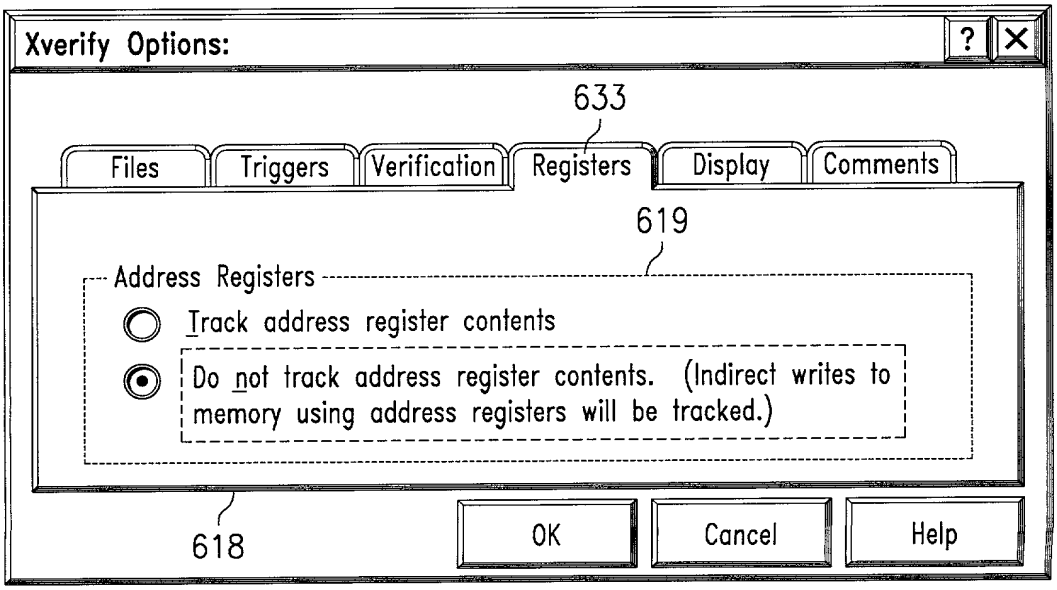

Xverify Options:
633
Files
Triggers
Verification
Registers
Display
Comments
619
Address Registers
Track address register contents
Do not track address register contents. (Indirect writes to memory using address registers will be tracked.)
618
OK
Cancel
Help

FIG. 6b

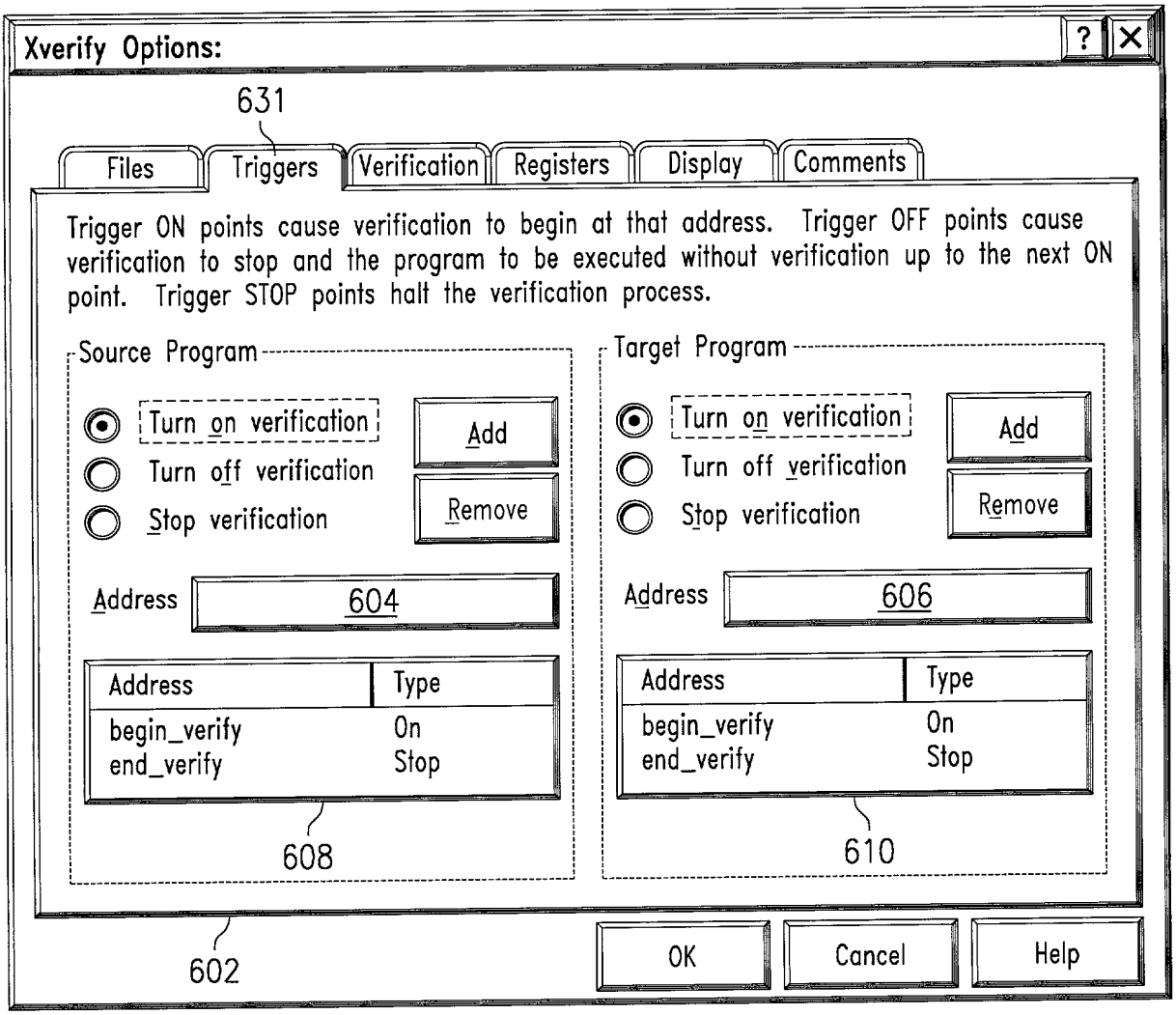

Xverify Options:
631
Files
Triggers
Verification
Registers
Display
Comments
Trigger ON points cause verification to begin at that address. Trigger OFF points cause verification to stop and the program to be executed without verification up to the next ON point. Trigger STOP points halt the verification process.
Source Program
Turn on verification
Turn off verification
Stop verification
Add
Remove
Address
604
Address
Type
begin_verify
On
end_verify
Stop
608
Target Program
Turn on verification
Turn off verification
Stop verification
Add
Remove
Address
606
Address
Type
begin_verify
On
end_verify
Stop
610
602
OK
Cancel
Help

FIG. 6f

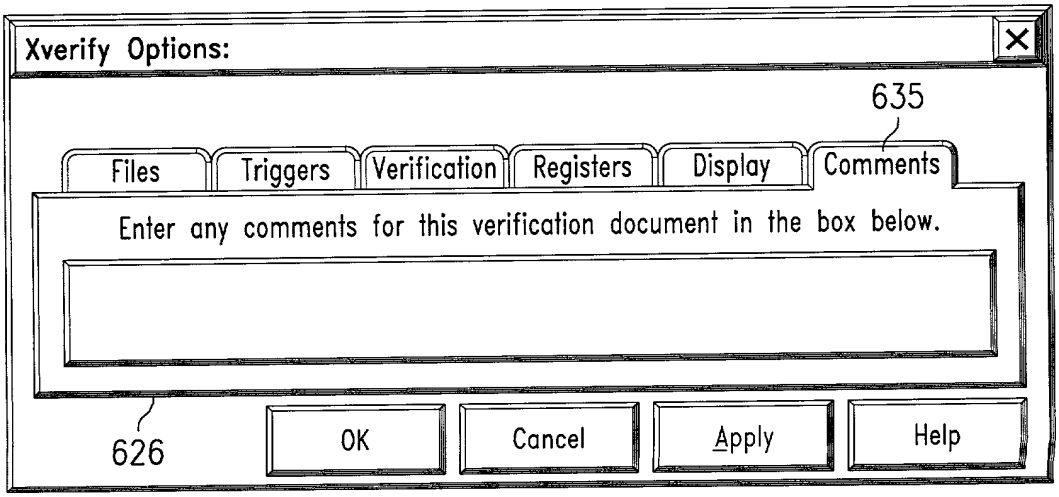

Xverify Options:
635
Files
Triggers
Verification
Registers
Display
Comments
Enter any comments for this verification document in the box below.
626
OK
Cancel
Apply
Help

FIG. 6c

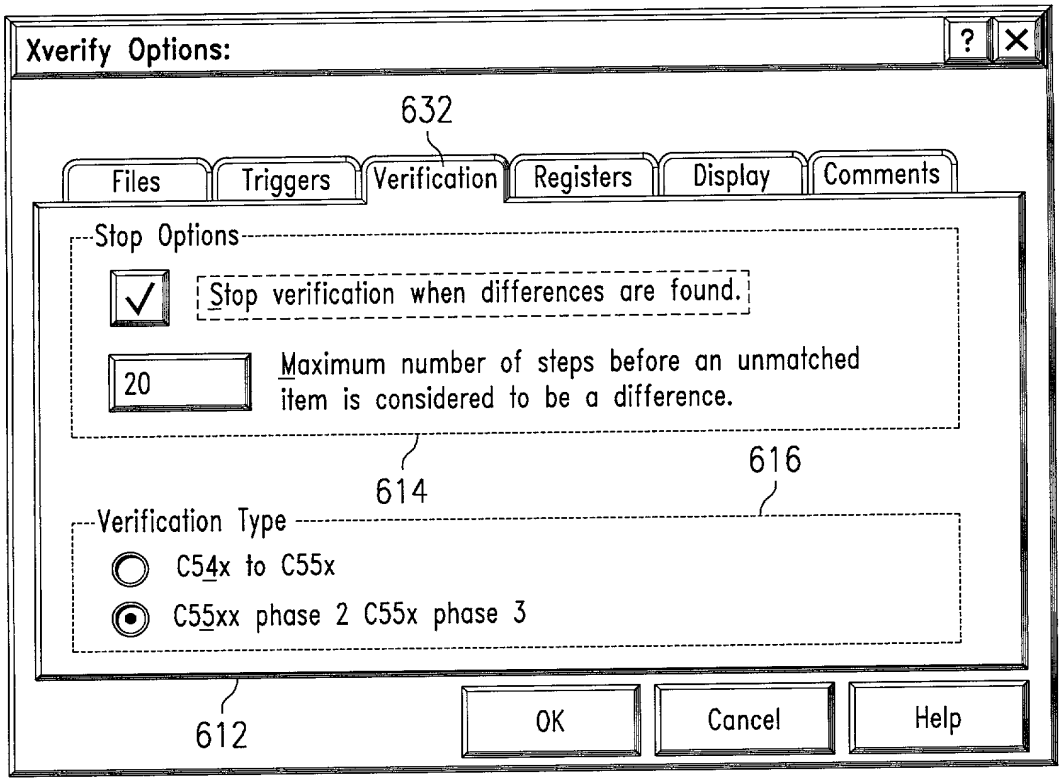


FIG. 6e

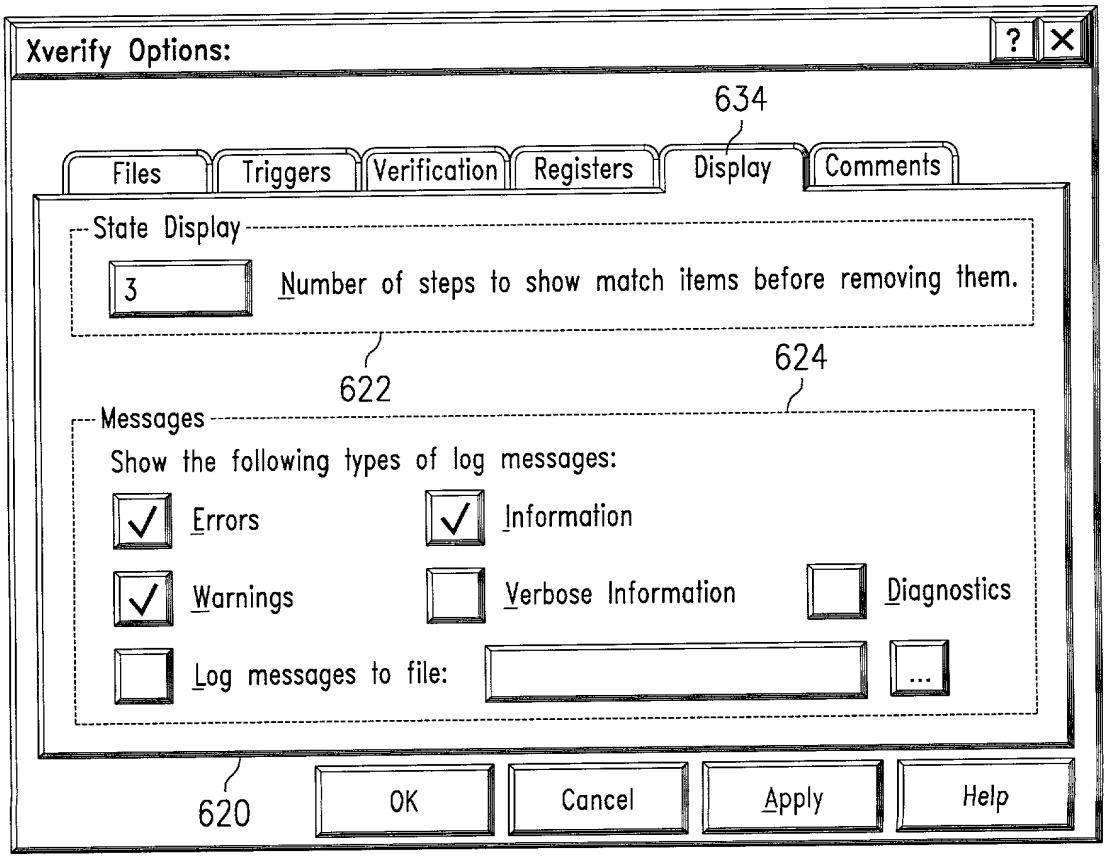
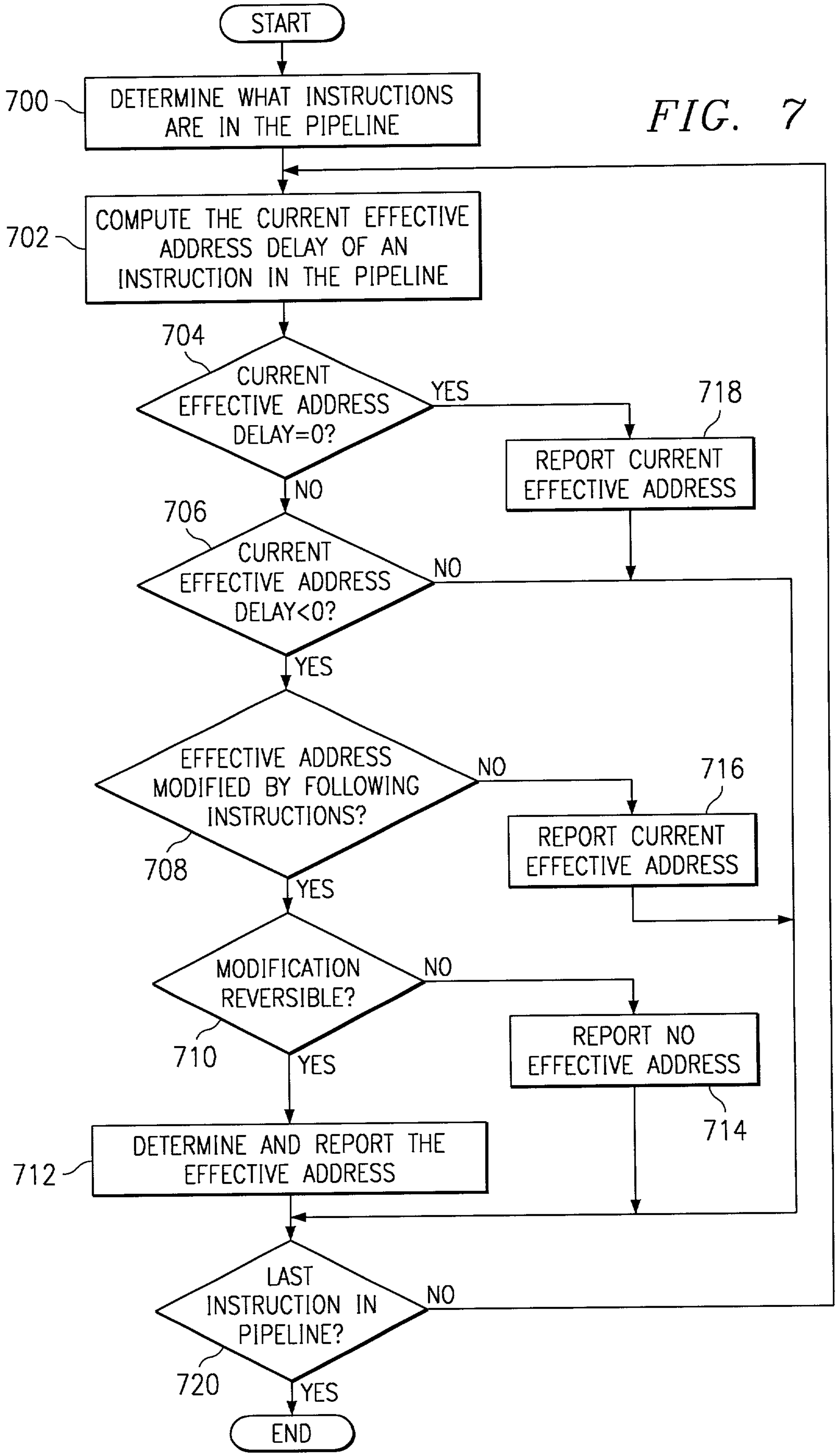


FIG. 7


START
700
DETERMINE WHAT INSTRUCTIONS ARE IN THE PIPELINE
702
COMPUTE THE CURRENT EFFECTIVE ADDRESS DELAY OF AN INSTRUCTION IN THE PIPELINE
704
CURRENT EFFECTIVE ADDRESS DELAY=0?
YES
718
REPORT CURRENT EFFECTIVE ADDRESS
NO
706
CURRENT EFFECTIVE ADDRESS DELAY<0?
NO
YES
EFFECTIVE ADDRESS MODIFIED BY FOLLOWING INSTRUCTIONS?
708
NO
716
REPORT CURRENT EFFECTIVE ADDRESS
YES
MODIFICATION REVERSIBLE?
710
NO
REPORT NO EFFECTIVE ADDRESS
714
YES
712
DETERMINE AND REPORT THE EFFECTIVE ADDRESS
LAST INSTRUCTION IN PIPELINE?
720
NO
YES
END